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VOLTAGE HARMONIC REDUCTION IN CAPACITIVE LOADS USING SYNCHRONOUS REFERENCE FRAME AND SPACE VECTOR PULSE WIDTH MODULATION

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ABSTRACT

Harmonics caused by capacitive loads were considered using the developed Shunt Active Power Filter (SAPF). The current harmonics are caused by the nonlinear characteristic of electronics-based equipment which increase power losses, and in turn reduce power quality. Switching signal generation was done using Space Vector Pulse Width Modulation (SVPWM). With an RC load under balanced input voltage conditions, the developed SAPF-SVPWM achieved a reduction of THD of 1.35% as compared to 35.46% before compensation. In addition, the developed SVPWM model was compared with SAPF without compensation using an RC load under unbalanced voltage conditions, and the results show that the developed SVPWM achieved a reduction in THD to 3.01% compared to 41.83% after compensation. The developed SVPWM model was also compared with Sinusoidal Pulse Width Modulation (SPWM) for balanced and unbalanced input voltage conditions. The results reveal that SVPWM performed better than SPWM. All the results obtained are within IEEE 519 harmonic limits with capacitive loads under balanced and unbalanced voltage conditions.

KEYWORDS

Balanced Voltage, Harmonics, Capacitive Loads, Unbalanced Voltage

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INTRODUCTION

The quality of utility supply is a major concern in electrical engineering due to the nonlinear characteristics of electronic appliances such as electrical drives, compact fluorescent lamps, and ovens, which inject harmonics into the distribution system (Soomro *et al.,* 2015). Poor power factor, voltage flicker, bad voltage regulation, voltage sags and swells are some examples of system disturbances. These issues result from the degradation of power quality caused by harmonics (Suleiman *et al.,* 2017; Suresh *et al.,* 2011). Harmonics also reduces the life span of electrical appliances and equipment, leading to significant economic losses in revenue (Suleiman *et al.,* 2017). A passive power filter is an effective way to reduce the harmonic current. However, the capability of a Passive filter to remove all the harmonic distortion at the point of coupling (PCC) is limited. Some drawbacks are bulkiness and frequency resonance with the inductor in the grid, which increases the harmonics (Sindhu *et al.,* 2015; Varaprasad *et al.,* 2014).

Recently, APF was introduced and accepted as one of the most common compensation methods. APF are switch mode power electronics inverters for harmonic cancellation at PCC so that harmonics-free load current is supplied to the consumers at PCC (Niklesh *et al.,* 2017). The strategies used to obtain the reference signal, switching, system topology and DC voltage determine the effectiveness of SAPF (Venkata *et al.,* 2014). Synchronous reference frame (d-q-o) theory, instantaneous real-reactive power (p-q) theory, modified instantaneous (p-q) theory, flux-based controller, notch filter; ANN etc. (Naresh *et al.,* 2012).

Synchronous Reference Frame (SRF) theory is widely used for reference signal generation owing to its directness, accuracy and dynamics compared to many other methods (Abhijit *et al.,* 2016). Similarly, hysteresis, triangular wave control, dead beat control, Space vector pulse width modulation (SVPWM), etc., have been confirmed in the literature for switching signal generation (Naresh *et al.,* 2012). SVPWM is known for its complexity and higher with rigorous mathematical requirements for switching generation (Phuong, 2012). SVPWM is one of the best signal generation because of the advantages of low switching loss, a wide modulation index range, and less distortion.

This work presents the development of SAPF. The synchronous reference frame is used for reference signal generation, and SVPWM is used for switching pulse generation. The paper is arranged as follows: Section 1 introduces the concept of SAPF. Section 2 details the mathematical equations of SAPF and SVPWM. Section 3 details the design procedure and implementation. Section 4 presents and discusses the obtained results, and Section 5 provides the conclusion.

SHUNT ACTIVE POWER FILTER (SAPF)

The idea of active power filters is to reduce the consumption of reactive power and harmonic currents in the power supply. The SAPF works by feeding the extracted harmonic currents in the opposing direction to the grid at the Point of Common Coupling (PCC). The effectiveness of an active power filter hinges on the method used to generate a reference current and the switching method used (Chelli *et al.,* 2015). The diagram of an SAPF is shown in Figure 1.

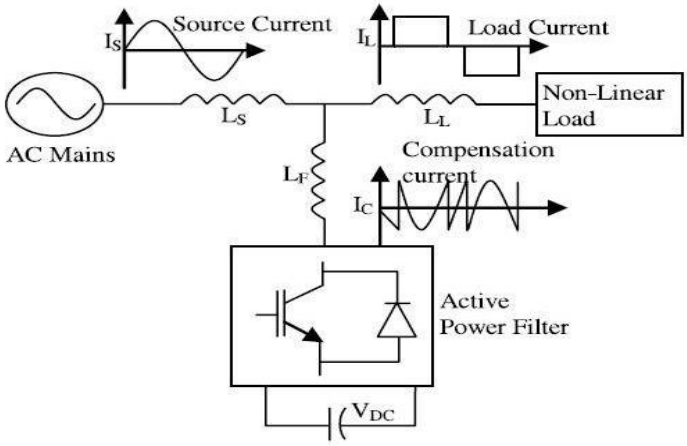

Figure 1: Block diagram of an SAPF

A. Synchronous Reference Frame (d-q)

The d-q theory transforms voltages and currents in a-b-c quantities into d-q as Dc quantities. Synchronous reference frame (d-q-0) theory transforms from a-b-c to (α-β) using Clark transformation equations and then transforms from (α-β) to (d-q-0) using Park transformation equations (Hemachandra *et al.,* 2015). The transformation equations are given as follows (Sunitha *et al.,* 2013).

B. Concept of Space Vector Pulse Width Modulation

Space vector pulse width modulation consists of six active sectors and two non-actives sectors with reference voltage vector $\vec{V}_{ref}$ which moves around the state vector. Figure 2 shows the reference voltage $\vec{V}_{ref}$ in sector one (Phuong, 2012).

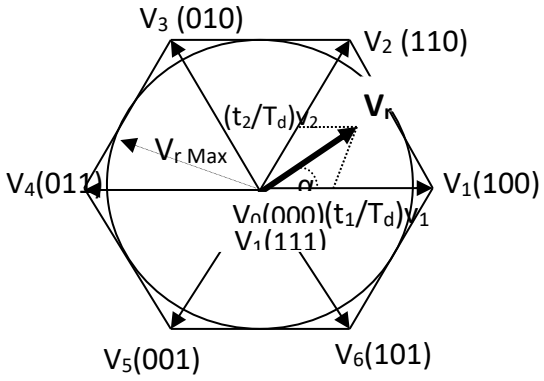

Figure 2: Space Vectors of Three-Phase Bridge Diagram

Table 1 shows the state of the switches when the reference voltage rotates around the sector (Phuong, 2012**)**.

Table 1: Switching States

Vector	State Switch	On Switch	Vector Definition
$\vec{V}_0$	[000]	S4, S6, S2	$\vec{V}_0 = 0$
$\vec{V}_1$	[100]	S1, S6, S2	$\vec{V}_1 = \frac{2}{3} V_{dc} e^{j0}$
$\vec{V}_2$	[110]	$S1, S3, S2$	$\vec{V}_2 = \frac{2}{3} V_{dc} e^{j\frac{\pi}{3}}$
$\vec{V}_3$	[010]	S4, S3, S2	$\vec{V}_3 = \frac{2}{3} V_{dc} e^{j\frac{2\pi}{3}}$
$\vec{V}_4$	[011]	S4, S3, S5	$\vec{V}_4 = \frac{2}{3} V_{dc} e^{j\frac{3\pi}{3}}$

$\overrightarrow{V_5}$	[001]	S4,S6,S5	$\overrightarrow{V}_5 = \frac{2}{3} V_{dc} e^{j\frac{4\pi}{3}}$
$\overrightarrow{V_6}$	[101]	S1,S6,S5	$\overrightarrow{V}_6 = \frac{2}{3} V_{dc} e^{j\frac{5\pi}{3}}$
$\overrightarrow{V_7}$	[111]	S1,S3,S5	$\overrightarrow{V}_7 = \frac{2}{3} V_{dc} e^{j\frac{6\pi}{3}}$

The line voltage $[V_{a\text{-}b}, V_{b\text{-}c}, V_{c\text{-}a}]$ is expressed in equation 2.

$$\begin{bmatrix} V_{a\text{-}b} \\ V_{b\text{-}c} \\ V_{c\text{-}a} \end{bmatrix} = V_{d\text{-}c} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \qquad (2)$$

Also, the phase voltage $[V_{a\text{-}n}, V_{b\text{-}n}, V_{c\text{-}n}]$ is expressed in equation 3.

$$\begin{bmatrix} V_{a\text{-}n} \\ V_{b\text{-}n} \\ V_{c\text{-}n} \end{bmatrix} = \frac{V_{d\text{-}c}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \qquad (3)$$

System Design and Modelling

A. Selection of DC Voltage, $V_{dc\text{-}ref}$

The minimum value of Vdc was calculated using equation 4

$$V_{dc} \geq \sqrt{3} V\text{pcc} - \max \qquad (4)$$

Vpcc-max = 400V

The required least of V_{dc} was calculated to be 693V. Therefore, 700V was chosen.

B. Selection of Coupling Inductor, L_f

The lowest value of the interfacing inductor was calculated using Equation 5

$$Lf \geq \frac{V_{dc}}{12fswI_{f\text{-}max}} \quad (5)$$

The converter maximum ripple current = 10A

Vdc = 693V (for modulation index = 1.7)

Switching frequency = 20 KHz.

The minimum value of L_f was calculated to be 2.88mH. Therefore, 3mH was chosen.

C. Selection of DC Capacitor, C_{dc}

The minimum value of the DC capacitor was calculated using Equation 6

$$C_{dc} = \frac{2S.n.T}{V_{dc\text{-}max}^2 - V_{dc\text{-}min}^2} = \frac{2S.n.T}{\{(1+z)V_{dc}\}^2 - \{(1-z)V_{dc}\}^2} = \frac{S.n.T}{2zV_{dc}^2} \quad (6)$$

The allowable compensator power transfer is 20kVA

Number of cycles, n is 0.5 (i.e., half cycle)

Period, T for one complete cycle is 0.02S

Change in Vdc of 10% (i.e. z = 0.1)

Vdc = 693V (for modulation index = 1.7)

The minimum capacity of Cdc was calculated to be 2082µF. Therefore, 3000µF was chosen.

D. SAPF Filter Modeling in d-q

The SRF method is implemented by transforming the three-phase source Va, Vb and Vc and load current i_a , i_b , and i_c into the three-phase (d-q-0) synchronous reference frame in DC quantities as follows (Mohammed, 2012):

$$L_f \frac{di_a}{dt} = V_{fa} - R_f i_{fa} - V_{sa} \quad (7)$$

$$L_f \frac{di_b}{dt} = V_{fb} - R_f i_{fb} - V_{sb} \quad (8)$$

$$L_f \frac{di_c}{dt} = V_{fc} - R_f i_{fc} - V_{sc} \quad (10)$$

Equations 5 to 7 are transformed to synchronous reference frame using the equation as expressed as follows:

$$L_f \frac{di_{fd}}{dt} = V_{fd} - V_{sd} - R_f i_{fd} - L_f \omega i_{fq} \quad (11)$$

$$L_f \frac{di_{fq}}{dt} = V_{fq} - V_{sq} - R_f i_{fq} + L_f \omega i_{fd} \quad (12)$$

The currents on the axes d and q are decoupled into two components as follows:

$$U_d = L_f \frac{di_{fd}}{dt} + R_f i_{fd} \quad (13)$$

$$U_q = L_f \frac{di_{fq}}{dt} + R_f i_{fq} \quad (14)$$

Therefore, equations 13 and 14 are re-written as expressed as follows:

$$V_{fd}^{*} = U_d + V_{sd} + L_f \omega i_{fq} \quad (15)$$

$$V_{fq}^{*} = U_q + V_{sq} + L_f \omega i_{fd} \quad (16)$$

Equations 15 to 16 are therefore modeled in Matlab/Simulink

E. Design of SVPWM

SVPWM can be implemented by the following steps (Jin-Woo, 2005)

(i) Determination of U_d, U_q, U_r and Angle θ

(ii) Determination of Time Duration T_0, T_1 and T_2

(iii) Transistors Switching Time Determination

F. Determination \of U_d, U_q, U_r and Angle θ

Determination of U_d, U_q, U_r and angle θ is derived as follows (Jin-Woo, 2005).

Consider the sector 1 of the space vector hexagonal diagram in Figure 3.

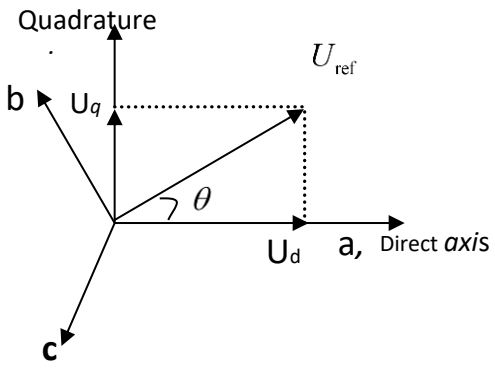

Figure 3: Space diagram in (d- q) Component

Direct voltage equation and quadrature voltage equation can be expressed as follows:

$$U_d = U_{a\text{-}n} - U_{b\text{-}n}\cos 60 - U_{c\text{-}n}\cos 60 \qquad (17)$$

$$U_q = 0 + U_{b\text{-}n}\cos 30 - U_{c\text{-}n}\cos 30 \qquad (18)$$

Equations 17 and 18 are also expressed as follows:

$$\begin{bmatrix} U_d \\ U_q \end{bmatrix} = 2/3 \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \quad (19)$$

Also, the equation of the alpha voltage and beta voltage is given as follows:

$$\begin{bmatrix} U_\alpha \\ U_\beta \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \quad (20)$$

Therefore, the reference voltage equation and alpha angle are written as follows:

$$|U_r| = \sqrt{U_\alpha^2 + U_\beta^2} \quad (21)$$

$$\theta = \tan^{-1}\left(\frac{U_\alpha}{U_\beta}\right) \quad (22)$$

Where:

θ is the angle between reference voltage and alpha voltage

Equations 19, 20, 21 and 22 were written as algorithms in Matlab function in Matlab function block in Matlab/Simulink to calculate U_d, U_q, U_r and angle θ

G. Determination of Time Duration T_{d0}, T_{d1} and T_{d2}

Consider the sector 1 of the space vector hexagonal diagram in Figure 4 (Naresh et al., 2012). The procedures for determining the switching time T_{d0}, T_{d1} and T_{d2} are illustrated as follows (Tej *et al.*, 2014; Raul, 2014).

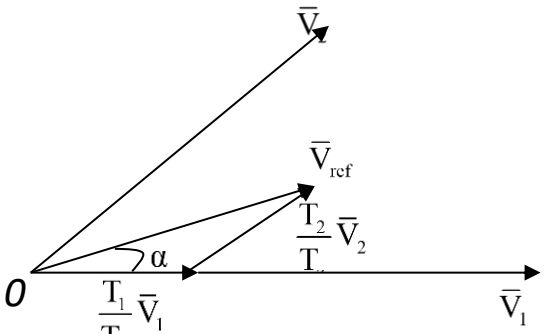

Figure 4: Reference Vector at Sector 1 (Naresh *et al.*, 2012)

The time of switching at any sector is therefore written as follows:

$$T_{d1} = \frac{\sqrt{3}T_d \left|\overline{U}_r\right|}{V_{d\text{-}c}} (\sin\frac{x}{3}\pi\cos\theta - \cos\frac{x}{3}\pi\sin\theta) \quad (23)$$

$$T_{d2} = \frac{\sqrt{3}T_d \left|\overline{U}_r\right|}{V_{d\text{-}c}} (\sin(\theta - \frac{x-1}{3}\pi)) \quad (24)$$

$$T_{d0} = T_d - T_{d1} - T_{d2} \quad (25)$$

Where:

x=1 (i.e., sector 1 -6) $\quad 0 \le \theta \le 60$

Equations 23, 24 and 25 will be written as algorithms in Matlab function in Matlab/Simulink for sector identification and to calculate T_{d0}, T_{d1} and T_{d2}

H. Transistors Switching Time Determination

Transistors switching time at each sector is computed in Table 2 (Dev, 2015).

Sector	Switches S1, S3, S5	SwitchesS4, S6, S2
1	$S1 = T_{d1}+T_{d2}+T_{d0}/2$ $S3 = T_{d2} + T_d/2$ $S5 = T_{d0}/2$	$S4 = T_{d0}/2$ $S6 = T_{d1}+T_{d0}/2$ $S1 =T_{d1}+T_{d2}+T_{d0}/2$
2	$S1 = T_{d1} + T_{d0}/2$ $S3 = T_{d1}+T_{d2}+T_{d0}/2$ $S5 = T_{d0}/2$	$S4 = T_{d2}+T_d/2$ $S6 = T_{d0}/2$ $S1 = T_{d1}+T_{d2}+T_{d0}/2$
3	$S1 = T_{d0}/2$ $S3 = T_{d1}+T_{d2}+T_{d0}/2$ $S5 = T_{d2}+T_d/2$	$S4 = T_{d1}+T_{d2}+T_{d0}/2$ $S6 = T_{d0}/2$ $S1 = T_{d1}+T_{d0}/2$
4	$S1 = T_{d0}/2$ $S3 = T_{d1}+T_{d0}/2$ $S5 =T_{d1}+T_{d2}+T_{d0}/2$	$S4 = T_{d1}+T_{d2}+T_{d0}/2$ $S6 = T_{d2}+T_d/2$ $S1 = T_{d0}/2$
5	$S1 = T_{d2}+T_d/2$ $S3 = T_{d0}/2$ $S5 = T_{d1}+T_{d2}+T_{d0}/2$	$S4 = T_{d1}+T_{d0}/2$ $S6 =T_{d1}+T_{d2}+T_{d0}/2$ $S1 = T_{d0}/2$
6	$S1 = T_{d2} + T_d/2$ $S3 = T_{d0}/2$ $S5 = T_{d1} + T_{d0}/2$	$S4 = T_{d0}/2$ $S6 = T_{d1}+T_{d2} + T_{d0}/2$ $S1 = T_{d2} + T_d/2$

Table 2: Sectors Transistors Switching Time Determination

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RESULTS AND DISCUSSION

Simulation of RC Load with Balanced Load (Balanced Voltage)

Figure 5 shows that the source current is not an ideal sinusoidal wave and is out of phase with input voltage due to the harmonic current generated by the RC load. The developed SAPF model was tested with the RC balanced load condition. Figure 6 shows the simulation waveforms of the developed SAPF. The results show that the source current (*Is*) is now an ideal sinusoidal wave and is in phase with the input voltage (*Vs*) compared to the waveform in Figure 5.

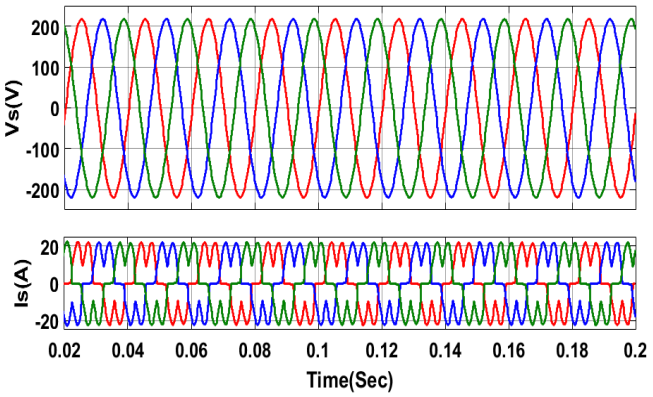

Figure 5: Waveforms of RC Load: Input Voltage (Vs), Source Current before Compensation

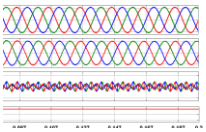

Figure 6: Simulation Waveform of RC Load after Compensation with SVPWM

Results of FFT Analysis of RC Load (Balanced Voltage)

The THD obtained in Figure 7 is 35.46%, and the fundamental (50Hz) value is 18.87A. This THD value is higher than the IEEE standard harmonic limit (i.e., < 5%). The developed SAPF model was subjected to Fast Fourier Transformation (FFT) analysis under balanced voltage conditions with SVPWM. The result obtained in Figure 8 shows the Fourier analysis of the load current after

compensation. The result shows a reduction of THD to 1.35% compared to 35.46% in Figure 7. Figure 9 shows the Fast Fourier Transform (FFT) analysis of the load current after compensation with SPWM. The results are within the IEEE harmonic standard limit of 5%.

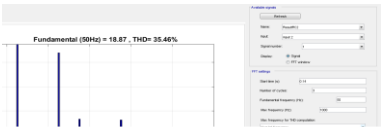

Figure 6: Fourier analysis of Source Current

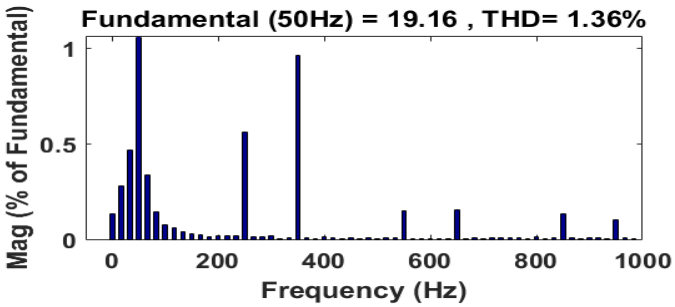

Figure 7: Fourier Analysis of Source Current (Is) with RC Load before Compensation

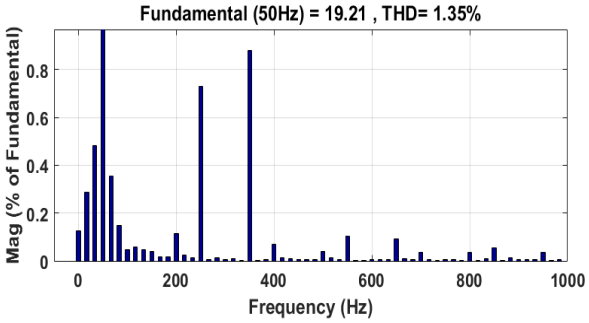

Figure 9: Fourier analysis of Source Current (Is) after Compensation with SVPWM for (Is) after Compensation with SPWM for RC Load RC Load

Simulation Result of RC Load (Unbalanced Voltage)

The developed SAPF model was tested with an unbalanced input voltage of $V_C = 220V$. Figure 10 shows the waveforms before and after applying the SAPF. The simulation waveform in Figure 10 shows that the source current is not an ideal sinusoidal because of the harmonic current generated by the combination of RC load and unbalanced voltage. The developed SAPF model was tested with RC balanced load condition. Figure 11 shows the simulation waveforms of the developed SAPF. The results reveal that, the source current (*Is*) is now sinusoidal and rotates with the same angle with the input voltage (*Vs*) when compared with Figure 10.

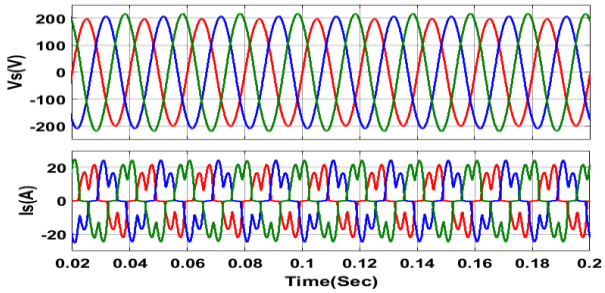

Figure 10: Waveforms of RC Load prior to Compensation

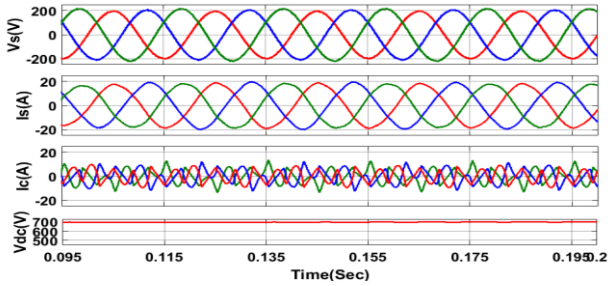

Figure 11: Waveform of RC Loads after Compensation

Result of FFT Analysis of RC Load (Unbalanced Voltage)

Figure 12 shows the Fourier analysis of load current before applying the developed model. The THD obtained in Figure 12 is 41.83 %, and the fundamental (50Hz) value is 16.09A. This THD value is larger than the IEEE standard harmonic limit (i.e., < 5%). The developed model was subjected to Fast Fourier Transformation (FFT) analysis under balanced voltage with SVPWM. The result obtained in Figure 13 shows the Fast Fourier Transformation (FFT) analysis of load current after compensation. The result shows a significant 3.01% reduction of THD compared to 41.83% in Figure 12. Figure 14 shows the Fast Fourier Transformation (FFT) analysis of load current after compensation with SPWM. The result is within the IEEE harmonic standard limit of 5%.

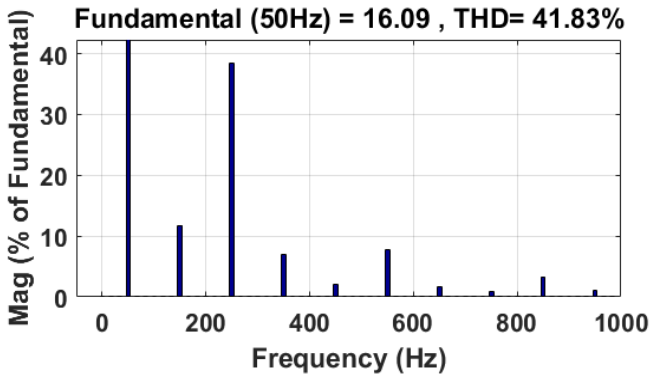

Figure 12: Fourier Analysis of Source Current (Is) with RC Load before Compensation

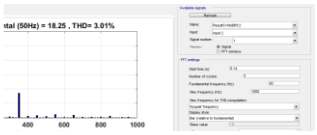

Figure 13: Fourier Analysis of the Source Current for RC (Is) after Compensation with SPWM for RC Load

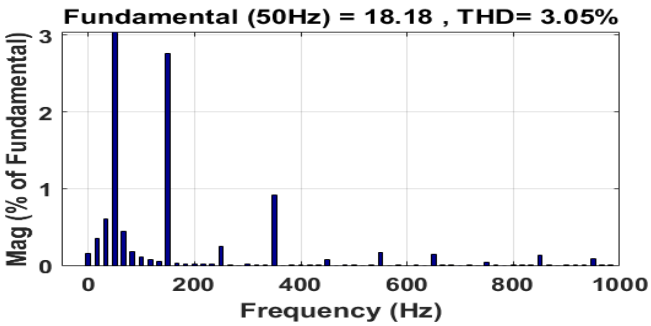

Figure 14: Fourier analysis of Source Current (Is) after Compensation with SVPWM Load

TABLE 2: RESULTS SUMMARY

CONCLUSION

The developed model was tested for both RC loads under balanced and unbalanced sinusoidal voltage input. FFT analysis shows that harmonic has been reduced from 35.460% to 1.35 % (THD) for RC nonlinear load for balanced load and 41.83% to 1.74% for unbalanced load using SVPWM. SPWM also reduced harmonic from 35.46% to 1.36% under a balanced RC load and 41.83% to 3.01% under an unbalanced RC load. The results reveal that SVPWM performed better than SPWM. The FFT analysis shows that all the results are within the limits of IEEE 519.

Voltage	**Control Strategy**	**THD without SAPF**	**THDs with SAPF**	
			SVPWM	**SPWM**
Balanced	SRF	35.46	1.35	1.36
Unbalanced	SRF	41.83	3.01	3.05

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